REMARKS

This application has been carefully reviewed in light of the Office Action dated March 18, 2004. Claims 1-7 and 12-18 remain in this application. Claims 1, 2, 4, 5, 7, 12, and 16 are the independent Claims. Claims 8-11 have been canceled without prejudice. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Allowable Subject Matter

On pages 2 and 3 of the Office Action, Claims 1-4 and 16-18 were indicated to be allowed.

Applicant thanks the Examiner and formally recognizes the allowable subject matter of Claims 1-4 and 16-18.

Art-Based Rejections

On page 3 of the Office Action, Claims 5, 7-8, and 12 were rejected under 35 U.S.C. §102(e) over U.S. Patent No. 5,801,674 (Shimizu). On page 5 of the Office Action, Claims 9-11 and 13-15 were rejected under 35 U.S.C. §103(a) over Shimizu in view of S-MOS System, Inc., Dot Matrix LCD Driver SED 1520/21 Version 1.0, October, 1996, (S-MOS). Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the arguments below.

The Shimizu Reference

Shimizu is directed to a driving device for driving a display device. (*See, Shimizu, abstract; Col. 1, lines 6-7*). Shimizu discloses a display device including a liquid crystal display panel having a plurality of scanning electrodes, a plurality of signal electrodes divided into a plurality of signal electrode groups, and liquid

crystal elements arranged at intersections of the scanning electrodes and the signal electrodes. (*See, Shimizu, Col. 2, lines 40-43*). According to Shimizu a controller is provided for outputting control signals including a start signal, enable signal and clock signal and display data; and a plurality of drivers supplied with the display data and the control signals including the start signal, enable signal and clock signal from the controller, for fetching the display data and selectively supplying the fetched display data to the plurality of signal electrode groups. (*See, Shimizu, Col. 2, lines 45-52; Col. 3, line 66 to Col. 4, line 18; Figure 1*).

The Claims are Patentable Over the Cited References

The present invention is generally directed to an electro-optical device using an electro-optical element.

As defined by independent Claim 5, an electro-optical device includes a display section which includes a plurality of first electrodes extending in a first direction, a plurality of second electrodes extending in a second direction crossing the first direction, and electro-optical elements driven by the first and second electrodes. A first driver drives the first electrodes. A second driver drives the second electrodes. The first driver has a master IC for driving a first group of the first electrodes and at least one slave IC for driving a second group of the first electrodes. The master IC includes a display control signal generation section which generates a display control signal based on a signal from an external MPU. An internal delay circuit delays the display control signal. An output terminal outputs the display control signal before the display control signal passes through the internal delay circuit. At least one slave IC has an input terminal for receiving the display control signal output from the output terminal of the master IC through an external wiring.

The applied reference of record does not disclose or suggest the above features of the present invention as defined by independent Claim 5. In particular, the applied reference does not disclose or suggest, "an internal delay circuit which delays the display control signal," as required by independent Claim 5.

The Office Action purports that the delay circuit 112a in Fig. 3 of Shimizu corresponds to the internal delay circuit of independent Claim 5. The Office Action further purports that the signal ENABLE E2 output from the terminal EO of Shimizu corresponds to the display control signal of independent Claim 5. However, Applicant respectfully traverses these inferences.

The delay circuit 112a of Shimizu does not meet the requirement to delay the signal ENABLE E2, as recited in independent Claim 5. According to Shimizu, the delay circuit 112a is provided in an input circuit 11 and data from the input circuit 11 is input to delay circuits 112a, 112b through buffers BF1 and BF2, flip-flop circuits FF11 and FF12, mask circuits (AND) 111a and 111b. *(See, Shimizu; Fig. 3; Col. 5, lines 18-65).* The delay circuit 112a of Shimizu delays input data and does not delay the display control signal, as required by independent Claim 5.

Shimizu discloses that the signal ENABLE E2 is input to one terminal of the previous stage mask circuit (AND) 111 in the delay circuit 112a. The signal ENABLE E2 is a low/high mask signal and is used for either masking display data received by another terminal of the mask circuit (AND) 111 or for letting the display data pass through. The effective output of the mask circuit (AND) 111 is the display data. Therefore, the delay circuit 112a of Shimizu delays display data supplied to the serial-parallel circuit 14 as shown in Fig. 2, but not the display control signal, as required by independent Claim 5. Shimizu provides the delay circuit 112 so as to set the output timing of the display data coincident with the operation timing of the other circuit. *(See, Shimizu; Col. 5, line 66 to Col. 6, line 4).*

In contrast, the internal delay circuit as required in independent Claim 5 serves to prevent the timing difference of the display control signal between the master IC and the slave IC. This reduces the luminance difference in a screen so as to improve image quality of a displayed image. *(See, Specification; Page 3, lines 1-6; Page 5, lines 16-22; Page 22, lines 1-12).*

The ancillary S-MOS reference is not seen to remedy the deficiencies of the primary Shimizu reference. In particular, S-MOS does not disclose or suggest the limitation of, "an internal delay circuit which delays the display control signal," as required by independent Claim 5.

Since the cited references fail to disclose, teach, or suggest the above features recited in independent Claim 5, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, independent Claim 5 is believed to be in condition for allowance, and such allowance is respectfully requested.

Applicant respectfully submits that independent Claims 7 and 12 are patentable over the cited references for at least the same reason as those discussed above with reference to independent Claim 5.

The remaining non-allowed claims depend either directly or indirectly from independent Claims 5, 7, and 12 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are, therefore, also believed to be in condition for allowance.

Conclusion

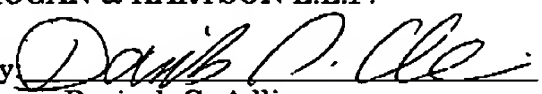
In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: July 16, 2004

By: 
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